APPLIED PHYSICS

Reconfigurable ferroelectric transistor array for embodied neuromorphic vision with hardware-native sensing, computing, and activation

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Edge artificial intelligence (AI) and embodied vision call for compact, fast, and energy-efficient hardware that integrates sensing, linear analog computation, and nonlinear activation, while flexibly reallocating these functions as workloads change. However, in-sensor computing (ISC) and in-memory computing (IMC) platforms still implement activation with external peripherals and use fixed functional partitions, which break the analog signal path and restrict system reconfigurability. Here, we report a reconfigurable ferroelectric transistor (Fe-FET) array in which polarization-programmed local fields enable junction-barrier engineering in ambipolar tungsten diselenide (WSe_2) channel. This junction-barrier engineering mechanism co-programs photoresponsivity, multilevel conductance, and tunable nonlinear transport within the same device, allowing each Fe-FET cell to be reassigned among weighted sensing (ISC), linear accumulation (IMC), and hardware-native activation. The array therefore functions as a uniform pool of physical units whose roles and spatial partitions can be dynamically allocated to match task demands without changing the hardware platform. Using this role-reconfigurable platform, we implement an end-to-end analog neuromorphic vision system in which broadband sensing, linear computation, and nonlinear activation are executed natively on the same Fe-FET platform. These results establish a task-adaptive and energy-efficient route toward scalable neuromorphic vision hardware for edge intelligence.

INTRODUCTION

The development of intelligent systems is driving demand for compact, low-latency, and energy-efficient edge hardware that integrates sensing, linear computation, and nonlinear activation with task-adaptive resource allocation (*1*–*5*). This demand is particularly acute for embodied platforms, including autonomous vehicles, mobile robots, and wearable agents, where stringent constraints on power, footprint, and response time make conventional sensor-memory-processor separation increasingly untenable (Fig. 1A) (*6*–*9*). In traditional architectures, raw sensory data must be shuttled across multiple hardware blocks and repeatedly converted between analog and digital formats, incurring substantial data-movement overhead, latency, and energy consumption (*10*–*14*). These bottlenecks have motivated device-level paradigms such as in-sensor computing (ISC) (*7*, *15*–*22*) and in-memory computing (IMC) (*23*–*31*), which execute analog operations directly within sensory (*7*, *23*) or memory elements (*32*–*34*), thereby reducing conversion steps and improving efficiency relative to von Neumann pipelines.

Despite rapid progress in ISC (*1*, *35*–*37*) and IMC (*23*, *38*–*40*) demonstrations at both device and array levels, a critical component of practical neuromorphic inference remains largely implemented outside the device plane (Fig. 1, B and C). Nonlinear activation functions (NAFs), such as rectified linear unit (ReLU) and sigmoid, are still commonly realized using digital logic (*41*–*45*) or complementary metal-oxide-semiconductor (CMOS) peripheral circuits (*46*–*49*). External implementation of activation interrupts the continuity of the analog processing chain and necessitates additional conversions and data movement, thereby reintroducing the latency and energy overhead that ISC and IMC aim to eliminate. It also constrains system-level configurability because changes in network depth, activation type, or task-specific signal conditioning often require extra peripheral circuitry and repeated remapping or system reconfiguration.

Prior efforts toward hardware nonlinearity have demonstrated activation-like responses in individual devices (*50*–*54*), yet a unified and reconfigurable physical platform that supports both linear mapping for weighted accumulation and programmable nonlinearity for activation within the same device remains a substantial challenge. Devices that emulate activation-like behaviors (e.g., ReLU or sigmoid) typically focus on nonlinear modulation alone (*54*–*57*) and do not provide controllable multilevel weight states required for linear computing. Conversely, mainstream analog-computing platforms, including memristors (*36*, *58*–*61*), ferroelectrics (*30*, *31*, *62*–*65*), and floating-gate memories (*2*, *45*, *62*, *66*, *67*), excel at analog storage and linear computing but generally lack a hardware-native and reconfigurable activation capability within the same physical unit. More broadly, most existing demonstrations achieve partial functionality through heterogeneous module assembly, where sensing, linear computation, and activation are realized by different components. The field

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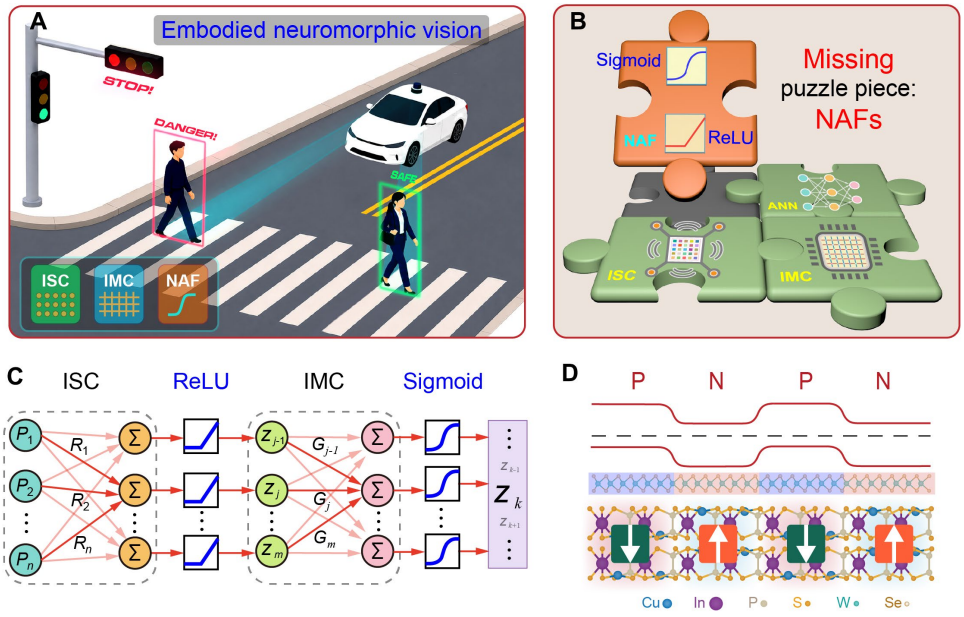

Fig. 1. Bridging the missing piece in neuromorphic vision systems: NAFs. (**A**) Conceptual illustration of embodied neuromorphic vision for autonomous driving. The inset highlights three core hardware primitives required for neuromorphic visual processing: ISC, IMC, and NAFs. (**B**) Schematic of the hardware system architecture depicted as a jigsaw puzzle. While ISC and IMC have been widely developed, NAFs such as ReLU and sigmoid are still commonly realized with peripheral digital logic or CMOS circuits, leaving a key gap for fully hardware-level neural processing. (**C**) Functional diagram of a typical neural network architecture with integrated ISC, IMC, and NAF stages. (**D**) Illustration of spatial polarization modulation using ferroelectric CIPS beneath the WSe_2 channel. The engineered in-plane junctions are formed by bipolar electrostatic doping driven by spatially programmed CIPS polarization. This enables reconfigurable control over photoresponsivity, channel conductance, and rectification behavior—forming the physical basis for tunable ISC, IMC, and NAF functionalities within a unified device platform.

therefore lacks a single device primitive that unifies these essential operations while enabling task-adaptive functional allocation within a uniform hardware platform.

Ferroelectric materials offer a promising route to such a primitive because remanent polarization generates nonvolatile internal electric fields that can reshape the electrostatic landscape and junction barrier profile (Fig. 1D) (*29*, *30*, *62*, *64*). When coupled to an ambipolar semiconductor, polarization-programmed local fields can, in principle, pattern carrier type and density along a channel and thereby create reconfigurable junction configurations. This physical capability suggests an opportunity to co-tune photoresponse, conductance states, and nonlinear transport within one device and to map these reconfigurable transport characteristics onto distinct neuromorphic roles.

Here, we establish a unified and reconfigurable ferroelectric transistor (Fe-FET) platform, where ferroelectric-induced local-field control enables fine-grained, programmable shaping of an in-plane junction barrier. Using two independently addressable split control gates, the polarization states of $CuInP_2S_6$ (CIPS) are programmed to generate spatially localized electric fields that electrostatically dope different segments of an ambipolar WSe_2 channel. This polarization-programmed junction-barrier engineering mechanism provides a unified physical control knob that dynamically and reversibly co-tunes multiple quantities, including photoresponsivity, multilevel conductance, and rectifying or highly nonlinear transport characteristics. As a result, the same Fe-FET can be reassigned among three essential neuromorphic roles, including ISC by photoresponsivity-coded sensory weights, IMC by conductance-coded linear accumulation, and hardware-native activation by programmable junction nonlinearity. This role reconfigurability turns a Fe-FET array into a pool of identical cells whose functions can be allocated on demand. The hardware can therefore adjust how many cells are devoted to sensing, linear accumulation, and activation according to task and layer requirements, reducing reliance on external activation peripherals and mitigating conversion and data-movement overhead. Building on this device primitive, we develop Fe-FET arrays and construct neuromorphic vision hardware that performs broadband sensing, linear analog computation, and nonlinear activation on the same reconfigurable platform. Representative tasks including classification, autoencoding, and embodied control are demonstrated, illustrating flexible functional assignment through polarization programming.

RESULTS

Mechanism of reconfigurable multifunctionality in the Fe-FET

A reconfigurable Fe-FET is developed as a single physical primitive for multifunctional processing in embodied neuromorphic systems. As illustrated in Fig. 2A, the device adopts a metal/ferroelectric/metal/insulator/semiconductor (MFMIS) structure, where a pair of laterally split CIPS capacitors are positioned beneath an ambipolar WSe_2 channel. These capacitors are gated independently by two multilayer graphene (MLG) electrodes (CG1 and CG2), which are patterned with a lateral separation of ~100 nm (fig. S1). This split-gate configuration enables spatially selective polarization programming, which generates nonvolatile, localized electric fields that electrostatically dope different channel segments and thereby shape the barrier profile of an in-plane junction within the WSe_2 channel. Details of the fabrication process are provided in Materials and

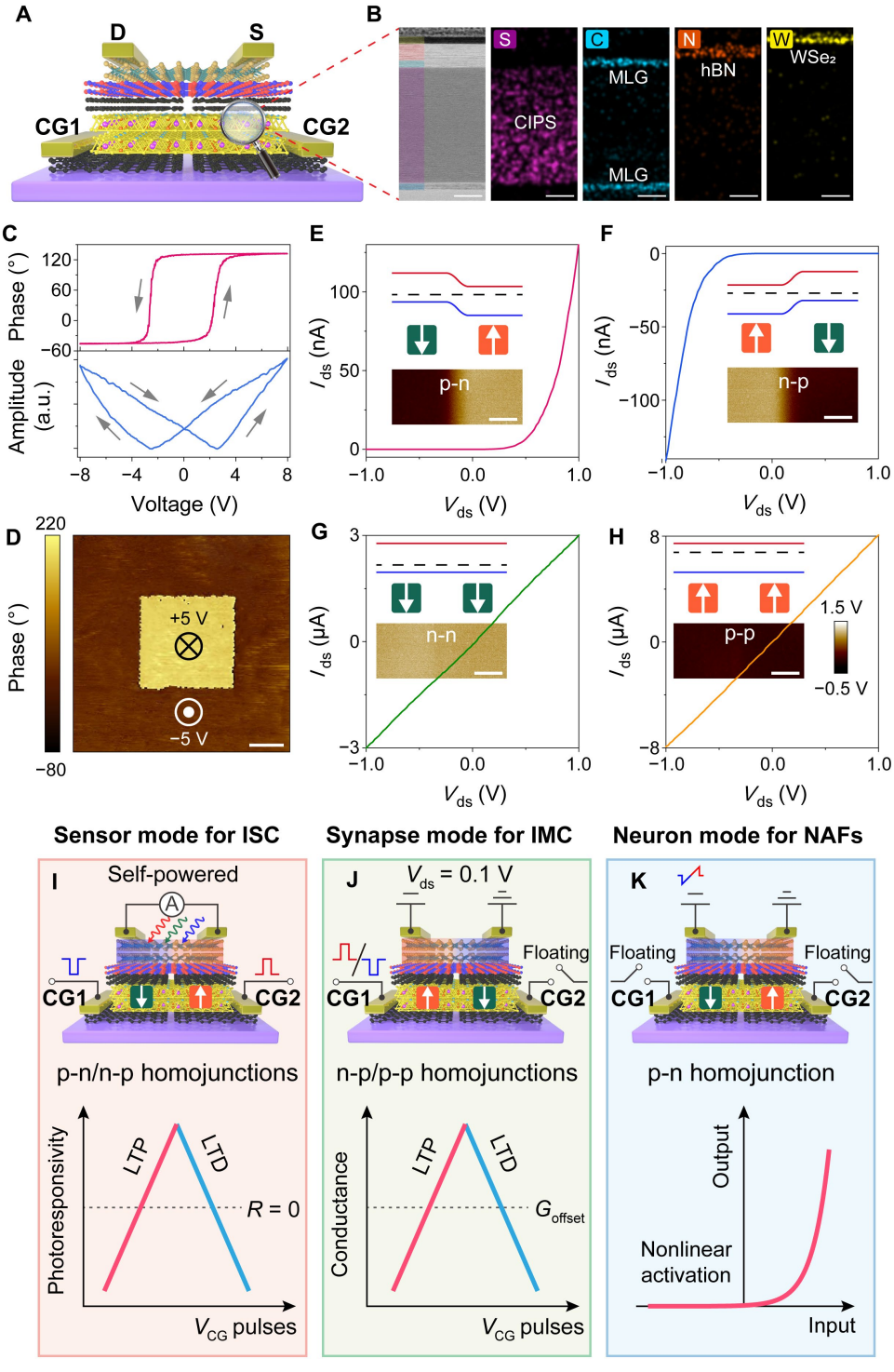

Fig. 2. Mechanism of reconfigurable multifunctionality in the Fe-FET. (**A**) Schematic illustration of the dual-gate Fe-FET, featuring two independently addressable MLG bottom gates (CG1 and CG2), split CIPS ferroelectric capacitors, and an ambipolar WSe_2 channel. (**B**) Cross-sectional STEM image and corresponding EDS elemental mappings showing well-defined interfaces among MLG, CIPS, hBN, and WSe_2 layers. Scale bars, 20 nm. (**C**) PFM amplitude and phase-voltage loops, exhibiting a butterfly-shaped response and a 180° phase reversal with a coercive voltage of ±2.5 V. (**D**) Out-of-plane PFM phase image after local voltage writing, demonstrating spatially resolved domain switching between +5 and −5 V regions. Scale bar, 1 μm. (**E** to **H**) Output characteristics of the Fe-FET under four homojunction states (p-n, n-p, n-n, and p-p), programmed via gate-selective polarization. Insets: Corresponding polarization configurations and spatial kelvin probe force microscope maps. Scale bars, 500 nm. (**I** to **K**) Configurations of the MFMIS operating for ISC (I), IMC (J) and NAF (K), respectively. a.u., arbitrary units. LTD, long-term depression. LTP, long-term potentiation.

Methods and fig. S2. Cross-sectional scanning transmission electron microscope (STEM) image and corresponding energy-dispersive spectrometer (EDS) mapping (Fig. 2B and fig. S3) reveal well-defined interlayer interfaces. Notably, the insertion of a bipolar graphene interlayer between the CIPS and hexagonal boron nitride (hBN) effectively compensates the depolarization fields (*68*), stabilizing the ferroelectric domains and enhancing device reliability.

The ferroelectric properties of CIPS were verified by piezoelectric force microscopy (PFM). The amplitude-voltage loop exhibits a characteristic butterfly shape, while the phase-voltage loop shows a 180° reversal under bipolar bias, confirming switchable polarization with a coercive voltage of ~±2.5 V (Fig. 2C). Out-of-plane PFM phase mapping further reveals stable up- and down-polarized domains after local voltage writing (Fig. 2D), confirming that the polarization state beneath each channel segment can be programmed nonvolatilely and reversibly (*68*, *69*). The polarization switching in CIPS involves a coupled mechanism of ferroelectric dipole reorientation and Cu-ion migration (*70*). Such ionic motion can locally modulate the electrostatic doping and contribute to the formation of reconfigurable p-n homojunctions in WSe_2, while the overall polarization remains nonvolatile and electrically reversible.

By independently controlling the polarization states of the left and right CIPS regions, the WSe_2 channel can be reconfigured into four in-plane junction configurations, i.e., p-n, n-p, p-p, and n-n. Each configuration exhibits stable and nonvolatile electrical characteristics (Fig. 2, E to H, and fig. S4), indicating that split-gate polarization programming reshapes the junction barrier height and asymmetry in a reproducible manner. The excellent retention across all four configurations is attributed to the robust room-temperature ferroelectricity of the CIPS layer (*71*) together with effective depolarization screening by the graphene interlayer. These results establish a ferroelectric-programmable junction-barrier engineering mechanism that provides a single physical control dimension for generating distinct device input-output characteristics.

This polarization-programmable junction-barrier device primitive directly underpins the multifunctional operation of the Fe-FET by enabling role reassignment of the same device cell. In sensor mode, the device is configured into a p-n or n-p configuration (Fig. 2I and note S1.1), where built-in fields drive self-powered photocurrent generation via the photovoltaic effect. Paired voltage pulses applied to CG1 and CG2 nonvolatilely and bidirectionally tune the photoresponsivity (fig. S5), allowing sensory weights to be encoded directly at the device plane for ISC. In synapse mode, the device operates in an n-p or p-p configuration (Fig. 2J and note S1.2), where multilevel conductance states are programmed nonvolatilely by gate pulses (fig. S6) and used as analog synaptic weights for IMC operations such as matrix-vector multiplication (MVM). In neuron mode, a programmable p-n junction yields rectifying and highly nonlinear current-voltage (I-V) characteristics with a tunable nonlinearity that spans ReLU-like to sigmoid-like responses (Fig. 2K), enabling hardware-native activation without peripheral circuitry (note S2). Collectively, these three functions are not realized by assembling separate device modules, but emerge as reconfigurable operating modes of the same ferroelectric-programmable junction-barrier device primitive.

Reconfigurable Fe-FET for linear ISC and IMC operations

Linear ISC and IMC in our platform are two role-specific realizations of the same ferroelectric-programmable junction-barrier device primitive. In ISC, the sensory weight is encoded in the programmed photoresponsivity of the in-plane junction, whereas in IMC, the synaptic weight is encoded in multilevel channel conductance. In both cases, polarization-programmed local electric fields reshape the junction barrier profile and thereby provide a unified physical basis for linear weighted operations at the device plane.

The Fe-FET operates as a self-powered photodiode for ISC when the in-plane junction is programmed into a p-n or n-p configuration. As shown in Fig. 3 (A and B), positive or negative short-circuit photocurrents (I_{sc}) are generated at the n-p/p-n interface with nanosecond-scale response speed (fig. S7). This sign-reconfigurable photovoltaic response originates from the polarization-defined built-in field across the junction, which drives photocarrier separation without an external bias. The polarization states of the split CIPS gates can be independently programmed by applying paired V_{CG} pulses with opposite polarity to CG1 and CG2, enabling continuous modulation of the junction state between n-p and p-n (fig. S5D). In this process, ferroelectric-induced local fields selectively dope the two channel segments and reshape the junction barrier, providing a single physical control dimension for analog weight tuning. By applying the sequential V_{CG} pulses as illustrated in fig. S8, the photoresponsivity can be programmed across 33 discrete levels within a dynamic range of ±160 mA W^{-1}, with excellent linearity and symmetry (Fig. 3C). The cumulative probability distribution of these levels across 1000 update events shows narrow, nonoverlapping variation (Fig. 3D), confirming high programming precision.

Compared to conventional Fe-FETs based on metal/ferroelectric/semiconductor (MFS) or metal/ferroelectric/insulator/semiconductor (MFIS) architectures, the MFMIS design used here suppresses depolarization effects and minimizes gate leakage (fig. S9) (*68*), substantially improving retention performance (fig. S10). This architecture is particularly important for linear ISC because it stabilizes the programmed local-field landscape that defines the junction barrier and the associated photoresponse weights. The programmed photoresponsivity levels remain stable over 10^4 s (Fig. 3E) and exhibit excellent endurance across 10^4 update cycles without degradation (Fig. 3F).

Beyond programmability, linear ISC hardware must maintain a consistent relationship between photocurrent and incident light intensity. The Fe-FET exhibits a highly linear I_{sc}-P dependence across all 33 photoresponsivity states over a broad optical power range (Fig. 3G), enabling accurate analog-analog multiplication. Figure S11 illustrates that the measured multiplication results closely match theoretical expectations. Further validation using 1000 optical pulses with randomly varied intensity confirms strong correlation between hardware output and expected response (fig. S12). Owing to the broad absorption of the WSe_2 channel, the Fe-FET supports broadband photodetection across the visible spectrum (fig. S13), making it suitable for multiband image processing. Notably, the ultralow dark current under short-circuit conditions allows direct accumulation of both positive and negative photocurrents without baseline correction (fig. S14), which simplifies downstream signal processing. Together, these results establish photoresponse-coded weighting as a linear operating mode that emerges from polarization-programmed junction shaping.

In addition to ISC, the Fe-FET supports linear IMC when configured into n-p or p-p configurations. In this mode, conductance states are modulated by applying voltage pulses to one of the gates (CG1), while the other remains fixed in a downward polarization state. Here, the programmed polarization-defined local field sets the background junction configuration, and the applied pulses further tune the junction barrier profile and channel carrier density,

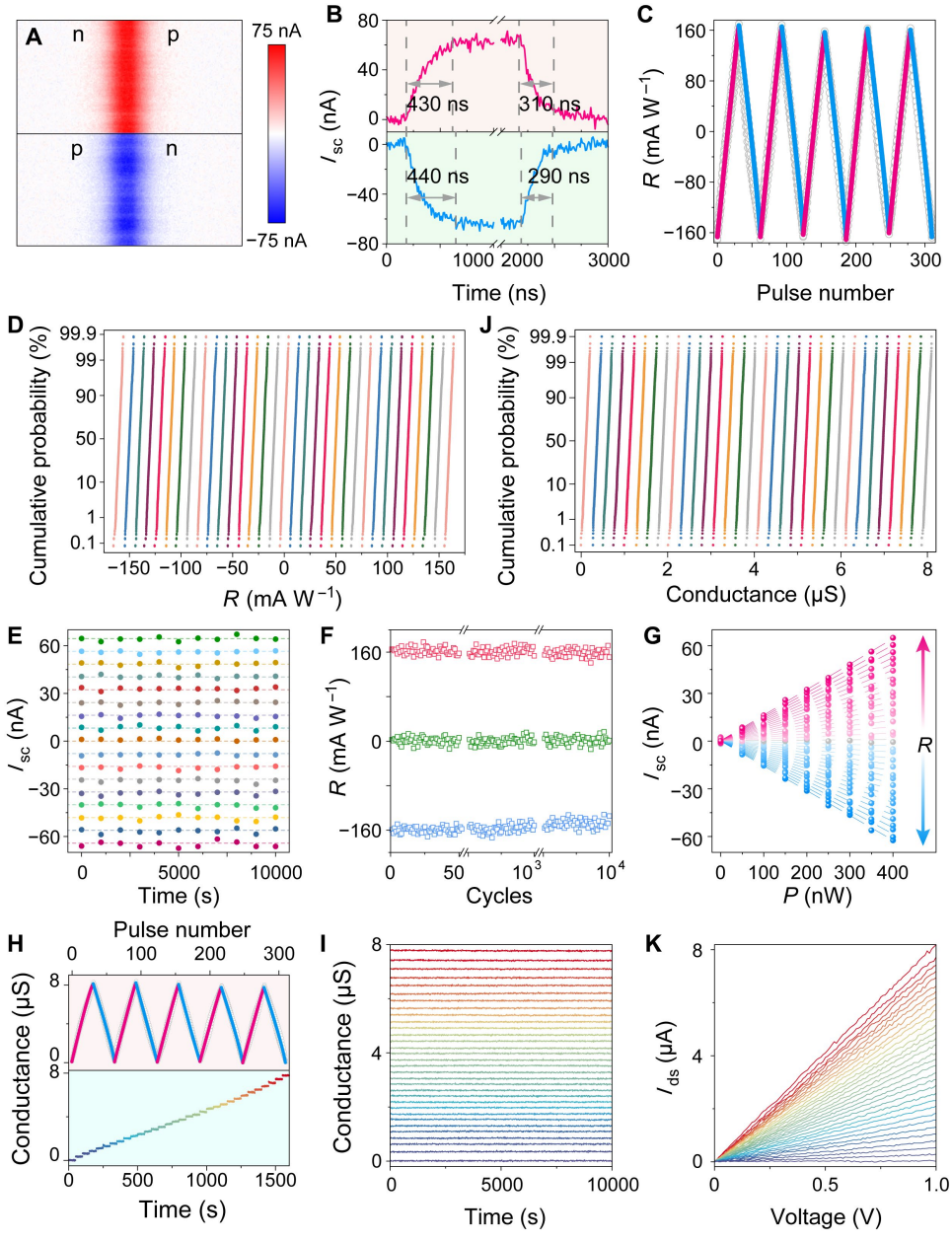

Fig. 3. Programmable and linear ISC/IMC characteristics of the reconfigurable Fe-FET. (**A**) Spatial photocurrent mapping of the Fe-FET in n-p (top) and p-n (bottom) configurations, showing polarity-dependent self-powered photoresponse. (**B**) Time-resolved short-circuit photocurrent (I_{sc}) signals under under pulsed illumination, with nanosecond-scale rise and fall times. (**C**) Linear and symmetric photoresponsivity (R) update between ±160 mA W^{-1} using sequential gate pulses. (**D**) Cumulative probability distribution of 33 discrete R states over 1000 update events, showing narrow and nonoverlapping distributions. (**E**) Retention characteristics of representative R levels monitored over 10^4 s. (**F**) Endurance performance of three R states across 10^4 programming cycles. (**G**) Light-intensity dependence of the photocurrents corresponding to all 33 photoresponsivity states. (**H**) Dynamic conductance (G) modulation via gate pulses under n-p or p-p configurations, yielding 32 programmable levels. (**I**) Nonvolatile retention of 32 discrete G states measured over 10^4 s. (**J**) Cumulative probability distributions of the G states across 1000 update cycles. (**K**) Output I-V characteristics corresponding to all 32 G levels, showing consistent linearity for IMC operations.

resulting in multilevel conductance states that serve as analog weights. As shown in Fig. 3H, the device conductance can be tuned across a wide range from 10 pS to 8 μS, spanning six orders of magnitude. Thirty-two discrete conductance levels exhibit robust retention (Fig. 3I), narrow distribution widths across 1000 update events (Fig. 3J), and stable endurance over 10^4 update cycles (fig. S15).

For accurate IMC operations, the output current must scale linearly with input voltage across all conductance states. As demonstrated in Fig. 3K, the Fe-FET exhibits strong I-V linearity across all 32 levels. Analog multiplication results from the product of input voltage and programmed conductance closely match ideal values (figs. S16 and S17), ensuring high computational accuracy. In synapse mode,

the device achieves an operation speed of 8 ns (fig. S18), supporting neuromorphic computing frequencies up to 125 MHz.

Reconfigurable Fe-FET for nonlinear activation operations

NAFs are essential components of neural networks. Algorithmically, hidden layers benefit from a nonsaturating activation that preserves signal dynamic range during feature extraction, whereas the output layer requires a bounded nonlinearity for probability-like readout. However, in most hardware ISC/IMC platforms, such activation functions are still implemented with peripheral digital logic or CMOS circuitry, which breaks the continuity of the analog signal pathway and limits system configurability. To address this gap, we show that the ferroelectric-programmable junction-barrier device primitive can generate hardware-native, programmable nonlinear input-output characteristics, enabling ReLU-like and sigmoid-like activations (note S2).

When programmed into a p-n junction configuration, the Fe-FET exhibits tunable rectifying and nonlinear *I-V* characteristics that can be mapped onto commonly used NAFs. To investigate this capability, we systematically examined how the polarization state of the CIPS layer affects the junction characteristics of the Fe-FET (fig. S21). As described in note S2, weak polarization produces a shallow junction barrier in the WSe_2 channel, yielding a nearly linear rectifying response under forward bias (Fig. 4A), which is well described by a ReLU-like activation behavior. In contrast, stronger polarization increases the effective barrier height and enhances transport nonlinearity, resulting in an S-shaped *I-V* characteristic (Fig. 4B) that is well described by a sigmoid-like activation behavior. Figure 4C presents the distribution of the transition voltage V_T, defined as the voltage at which the *I-V* curve transitions from a strongly nonlinear regime to an approximately linear regime. A smaller V_T corresponds to an earlier onset of the quasilinear region and is desirable for ReLU-like activation, whereas a larger V_T preserves nonlinearity over a broader voltage range and supports sigmoid-like responses. This polarization-tunable V_T provides a direct and compact programming knob for selecting and tuning activation behavior within the same device cell. The Fe-FET achieves a response time of ~8 ns in NAF mode (fig. S26), supporting fast inference in neuromorphic systems.

To validate its applicability in neural networks, we implemented a 4 × 4 Fe-FET array as a nonlinear activation module within a convolutional neural network (CNN) (Fig. 4, D and E). In this system, ReLU-like and sigmoid-like activations are physically realized by polarization-programmed Fe-FET cells for the hidden and output layers, respectively, without auxiliary digital activation circuitry.

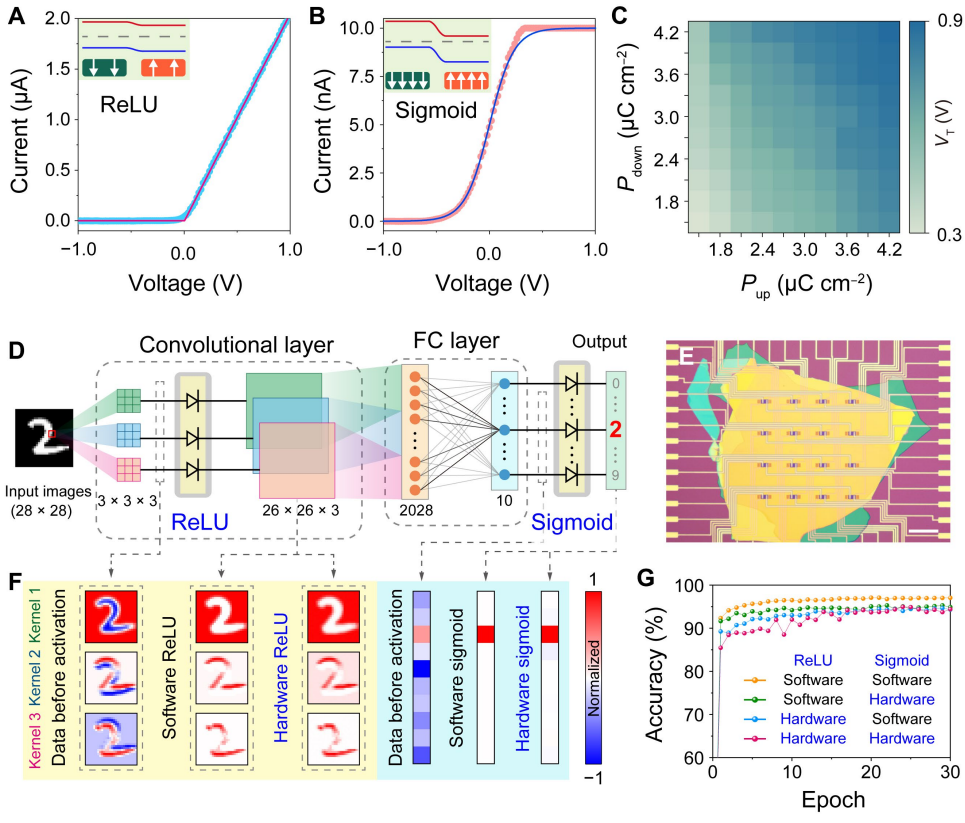

Fig. 4. Single-device implementation of reconfigurable ReLU and Sigmoid activation in Fe-FETs. (**A** and **B**) Representative *I-V* characteristics of the Fe-FET configured for ReLU-like (A) and sigmoid-like (B) activation behaviors under different CIPS polarization states. The solid lines represent the ideal ReLU and sigmoid curves. Insets illustrate corresponding polarization configurations of CIPS and band alignments of WSe_2 channel. (**C**) Heatmap of the transition voltage V_T as a function of CIPS polarization states (P_{up} and P_{down}), extracted from the *I-V* curves in fig. S20. (**D**) Schematic of the CNN architecture for MNIST classification, with Fe-FETs integrated as hardware ReLU and sigmoid units in the convolutional and output layers, respectively. (**E**) Optical image of the 4 × 4 Fe-FET array used for hardware activation. Scale bar, 30 μm. (**F**) Activation maps generated by software and hardware ReLU/sigmoid functions, showing close agreement in spatial outputs. (**G**) CNN classification accuracy under different activation configurations. The Fe-FET–based hardware activation achieves 95% accuracy, closely matching the software benchmark (97%).

Figures S36 to S39 confirm consistent device performance under both activation modes. As shown in Fig. 4F, the output currents from the hardware closely match those predicted by software activation functions. As a result, the hardware-accelerated CNN achieves a classification accuracy of 95% on the Modified National Institute of Standards and Technology (MNIST) dataset, approaching that of the software baseline (97%) (Fig. 4G and fig. S46).

Notably, the Fe-FET is not limited to ReLU- and sigmoid-like activations. Further experiments show that, by more finely programming the p-n junction barrier and using minimal auxiliary circuitry, more complex activations such as Mish, leaky ReLU, and a Softmax building block can also be implemented (fig. S25).

End-to-end neuromorphic vision hardware enabled by reconfigurable Fe-FET arrays

The multifunctional Fe-FET platform enables a hardware-native neuromorphic vision dataflow on a unified hardware platform, with task-adaptive role allocation across identical, reconfigurable cells. The key operations of a neural network, including sensory encoding, linear accumulation, and nonlinear activation, are implemented directly in hardware using reconfigurable Fe-FET arrays. Optical stimuli are converted into analog photocurrents in the sensor array, and sensory weights are encoded as programmable photoresponsivity to enable in-sensor weighted sensing. Linear weighted accumulation is carried out using conductance-coded states for matrix-vector operations, while nonlinear transformations are executed through polarization-programmable junction-barrier nonlinearity. As shown in Fig. 5A and fig. S48, the system architecture is constructed entirely from Fe-FET arrays configured to operate in three neuromorphic modes: ISC, IMC, and NAFs. A $3 \times 3 \times 3$ array and a 3×9 array are used for ISC and IMC tasks, respectively, while a 4×4 array is dedicated to NAF operations (Fig. 5B). All three neuromorphic functions are realized at the device level, forming a reconfigurable hardware platform that can dynamically assign sensing, linear accumulation, and nonlinear transformation according to task and layer requirements. Details of the array-level uniformity and system architecture analysis are provided in notes S3 and S4.

To demonstrate the real-time processing capabilities of this system, we first validated multiband convolutional operations directly in the ISC module. The Fe-FET's broadband photoresponse enables simultaneous image sensing and filtering within the same hardware layer. As shown in fig. S45, spatial filters including Sobel and Laplacian kernels were implemented by programming photoresponsivity maps across the ISC array and applied to images spanning the 400- to 800-nm wavelength range. The resulting output feature maps closely match software results, confirming accurate and scalable in-sensor convolution.

We next evaluated supervised classification using a custom dataset of noise-added symbolic patterns ("┐," "┌," and "┬") (fig. S52). Analog output currents generated by the ISC array (fig. S49) were directly processed by polarization-programmed sigmoid-type Fe-FET activators, yielding activation values f_1, f_2, and f_3 (Fig. 5C) corresponding to classification probabilities (see Materials and Methods for details). The system converged within several training epochs (Fig. 5D), and the learned optical-electrical weights (photoresponsivity states) were retained nonvolatilely in the ISC module (figs. S53 and S54), enabling zero-standby-power inference. To further verify hardware-native decision-making, the trained Fe-FET classifier was integrated into a mobile robotic platform. As shown in fig. S55, traffic-like symbols were optically projected onto the ISC array, and the resulting hardware-level classification outputs directly issued movement commands (left, right, stop), establishing a closed-loop percept-compute-actuate cycle entirely powered by monolithic Fe-FET arrays. Further demonstrations using 32×32–pixel images from the Kaggle Traffic-Signs Dataset are provided in Materials and Methods and figs. S56 to S59.

The integration of sensing, linear computation, and nonlinear activation within a single device enables task-adaptive role allocation. A single Fe-FET array can be treated as a pool of identical, reconfigurable cells whose roles are reassigned on demand, allowing the hardware to dynamically adjust how many cells are devoted to ISC, IMC, and activation as task complexity changes. As a demonstration, we used the neuromorphic vision hardware to perform fully analog, real-time processing of University at Albany Detection and Tracking (UA-DETRAC) traffic video streams with dynamic role reconfiguration (Fig. 5E). Owing to the limited available array size, the full neural-network model (fig. S60) cannot yet be mapped at full scale in a single, fully parallel on-chip deployment. Instead, we adopted a task-slicing strategy and extracted three representative slices from the complete model (fig. S61). Each slice retains both linear computation and nonlinear activation, but differs in computational load and dataflow requirements (Fig. 5F). All three slices faithfully execute their intended computations, producing hardware outputs consistent with the software targets (Fig. 5G). Using the parameters extracted from these slices, we performed a system-level simulation of a scaled Fe-FET array and benchmarked it against a conventional von Neumann pipeline, projecting microsecond-level end-to-end latency and hundred-of-nanojoule-level per-frame energy (Fig. 5H), while maintaining ~98% accuracy comparable to the ~99% software baseline (Fig. 5I). Details are provided in Materials and Methods.

Beyond supervised classification, we further assessed the platform's capability for unsupervised analog learning. A full-hardware autoencoder was constructed, in which the ISC and IMC arrays served as encoder and decoder, respectively, with ReLU- and sigmoid-type Fe-FETs inserted as nonlinear activation units. As illustrated in fig. S62, images sensed by the ISC layer were encoded, activated, and decoded entirely within the analog hardware pipeline, reconstructing 3×3–pixel images with enhanced contrast and effective denoising (details in Materials and Methods). The system maintained high reconstruction fidelity over 5 hours (fig. S64), and hardware-generated outputs closely matched software baselines (structural similarity index, SSIM = 0.99).

DISCUSSION

To quantitatively assess the advantages of our reconfigurable Fe-FET platform, we compared its performance with representative ferroelectric-based devices (table S1). Benefiting from the low-barrier polarization switching of CIPS and the MFMIS architecture, the Fe-FET achieves 100-ns switching and stable nonvolatility across multiple states. Beyond device-level metrics, the central advance of this work lies in establishing a single reconfigurable device-level building block in which ferroelectric-programmable local fields enable junction-barrier engineering and thereby co-program photoresponsivity, multilevel conductance, and nonlinear transport within one device. This unified physical mechanism enables the same Fe-FET cell to realize the key operations required by neuromorphic vision

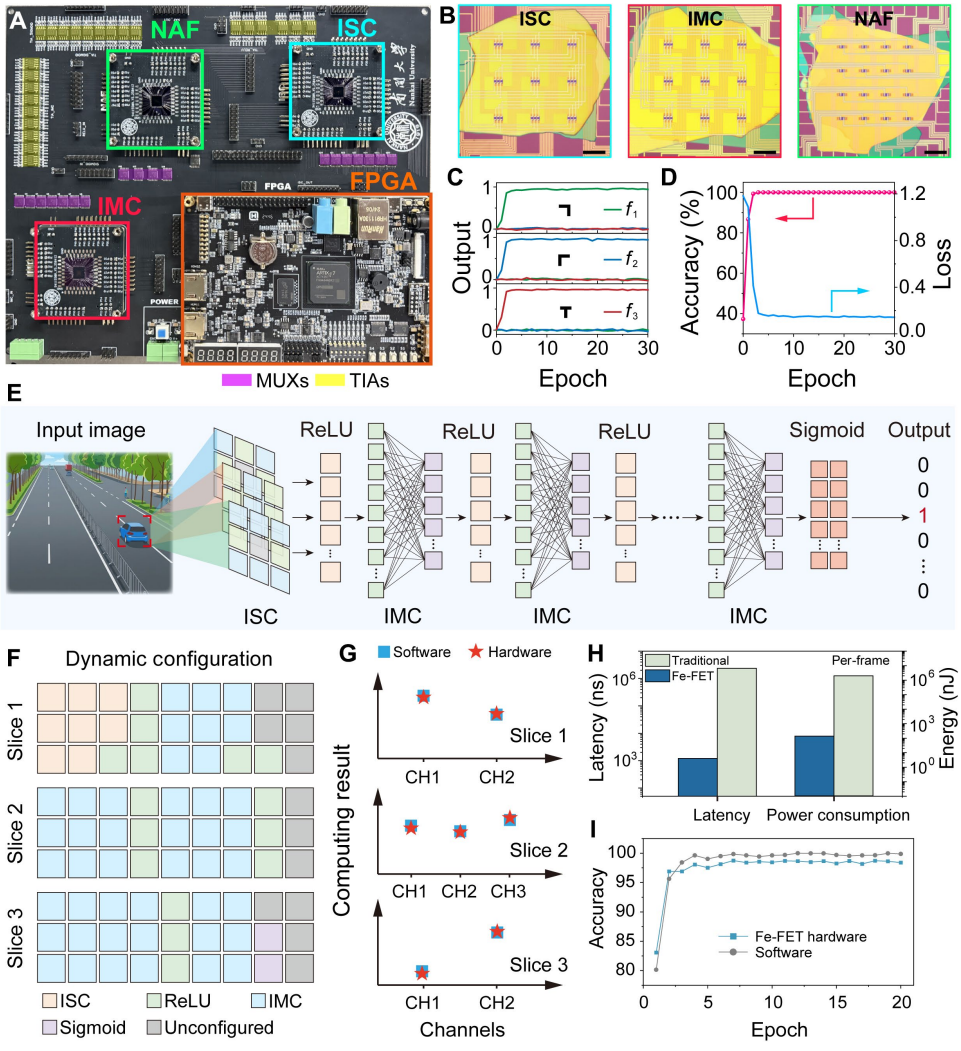

Fig. 5. Task-adaptive, end-to-end neuromorphic vision hardware enabled by reconfigurable Fe-FET arrays. (**A**) Photograph of the PCB-level validation platform integrating Fe-FET arrays (ISC, IMC, and NAFs) with peripheral circuitry (MUXs, TIAs, and FPGA). (**B**) Optical images of functional Fe-FET arrays for the ISC (left), IMC (center), and NAF (right) modules. The self-powered ISC array parallels devices with the same subpixel index for three independent photocurrent outputs (fig. S41). The 3 × 9 IMC synapse matrix applies three ReLU-derived input voltages (V_1–V_3) to word lines, collecting nine output currents (I_1–I_9) on shared bit lines (fig. S42). NAF arrays are programmed to ReLU or sigmoid via CIPS polarization; devices are individually addressed by preceding TIA outputs (TIA_{ISC} and TIA_{IMC}), with currents converted to voltages by TIAs for downstream processing. Scale bars, 30 μm. (**C**) Output currents (f_1 – f_3) from sigmoid-type NAFs in response to input patterns (┐, ┌, and ┬) during supervised training, indicating classification probabilities. (**D**) Evolution of classification accuracy and loss over 30 training epochs using the Fe-FET hardware. (**E**) Schematic of the neural-network model for traffic-video processing executed on the reconfigurable neuromorphic vision hardware integrating ISC, IMC, and NAFs. (**F**) Task-adaptive dynamic role allocation on the same physical array, demonstrating reprogrammed spatial partitioning for task slices with different computational loads. (**G**) Analog computation fidelity across three task slices, comparing software targets (blue squares) and hardware results (red stars) in representative output channels. (**H**) Benchmark of per-frame latency and energy for the Fe-FET pipeline versus a conventional separated (von Neumann–style) vision pipeline, showing reduced end-to-end latency and energy per frame enabled by local analog processing and minimized data movement. (**I**) Recognition accuracy on the UA-DETRAC traffic dataset, where the reconfigurable Fe-FET hardware achieves ~98% accuracy, comparable to the software baseline (~99%).

system, rather than combining separate devices that each perform only one function. Previous studies typically demonstrated only one or two of ISC, IMC, and activation, and NAFs were often implemented using heterogeneous components or peripheral CMOS circuitry (table S2). In contrast, the Fe-FET arrays implement sensory encoding, linear weighted accumulation, and nonlinear activation directly in hardware using the same device platform. This capability arises because polarization-programmed junction-barrier engineering allows each cell to be reassigned among ISC, IMC, and activation modes, providing task-dependent and layer-dependent functional allocation without introducing external activation circuits. As a result, linear mapping and programmable nonlinearity, which are fundamentally distinct operations in neural networks, are fused at the device-primitive level and can be invoked on demand by electrical programming. At the system level, this role-reconfigurable substrate enables a continuous analog processing pathway from sensing to decision, which reduces dependence on repeated format conversion and data movement. Moreover, the platform supports in situ weight

programming and adaptive reconfiguration at the device plane, eliminating repeated weight loading from external memory for the demonstrated tasks. Although the present prototype uses a micrometer-sized CIPS flake, the underlying junction-barrier–programmable concept can in principle be implemented with other scalable ferroelectric materials and device stacks (fig. S65), providing a practical path toward larger arrays and wafer-level neuromorphic hardware networks.

In conclusion, we present a reconfigurable Fe-FET array that unifies ISC, IMC, and NAF functionalities within a single physically reconfigurable device platform. By using polarization-programmed junction-barrier engineering as a shared physical mechanism, each Fe-FET can dynamically assume sensing, linear-computing, or nonlinear-activation roles, enabling task-dependent functional assignment on a compact and continuous analog signal pathway. Through array-level integration of these reconfigurable primitives, we demonstrate an end-to-end neuromorphic vision system where the same Fe-FET array can be reprogrammed to flexibly reassign cells among ISC, IMC, and NAF elements as task or layer demands change, enabling workload-adaptive resource use without altering the hardware platform. The proposed architecture provides a scalable, energy-efficient, and task-adaptable platform for future edge artificial intelligence (AI) systems and physically embodied intelligent agents.

MATERIALS AND METHODS

Fabrication of MFMIS-structure Fe-FET array

The fabrication process of the MFMIS-structure Fe-FET device array is illustrated in fig. S2. MLG (4.8 nm) was mechanically exfoliated onto a SiO_2/Si substrate and patterned into a 3 × 3 × 3 array using femtosecond laser micromachining. Each MLG flake was then split into two parts by focused ion beam cutting to define dual control gates (CG1 and CG2) with an intergate spacing of 100 nm. Cr/Au (10 nm/50 nm) electrodes were deposited using electron beam lithography (EBL) and evaporation to form electrical contacts to the MLG. A ferroelectric CIPS flake (~80 nm) was then transferred atop the patterned MLG to uniformly cover the gate array. Next, another exfoliated MLG flake (4.5 nm) was patterned into a split-square 3 × 3 × 3 array and precisely aligned on the CIPS layer using micromanipulation, overlapping with the underlying control gates. A dielectric hBN flake (~13 nm) was stacked to encapsulate the MLG/CIPS/MLG heterostructure. Last, a prepatterned ambipolar WSe_2 flake (~5 nm) was transferred atop the hBN to serve as the transistor channel, followed by deposition of Cr/Au (10 nm/50 nm) source and drain electrodes on the WSe_2 using EBL and evaporation. The precise alignment and stacking of the prepatterned two-dimensional material arrays were performed using a high-precision transfer and stacking platform (WeDo Tech, www.wedo-tech.com.cn).

Measurement setup

The fundamental electrical characteristics of the Fe-FET devices were measured using a semiconductor parameter analyzer (Keithley 4200A-SCS) equipped with a pulse measurement unit. Nanosecond-scale gate pulses for device reconfiguration and weight programming were generated by an arbitrary waveform generator (Tektronix AFG31052). Photocurrent maps of the devices, including those based on p-n and n-p homojunction configurations, were obtained using a WITec Alpha 300RAS scanning photocurrent microscopy module. For optical input experiments, laser sources at designated wavelengths were modulated by a spatial light modulator (SLM) operated in intensity-modulation mode. The resulting optical images were downscaled to 150 μm by 150 μm through a microscope objective and then projected onto the 3 × 3 × 3 Fe-FET array configured in sensor (ISC) mode.

Implementation of image classification on hardware neuromorphic vision system

The image classification task was implemented on the Fe-FET–based hardware neuromorphic vision system using a custom dataset composed of symbolic patterns (┐, ┌, and ┬) with added Gaussian noise (σ = 0.3; fig. S52). Each image had a resolution of 3 × 3 pixels and was randomly generated for both the training and test sets. The 3 × 3 × 3 device array is divided into 3 × 3 pixels, and each pixel consists of three subpixels. ISC operations were performed by electrically connecting devices sharing the same subpixel index (m = 1, 2, 3) in parallel across each pixel, thereby accumulating photocurrent outputs from the subpixels (fig. S49). The initial photoresponsivity values (weights) of the ISC devices were randomly assigned (fig. S44). During each training epoch, an input image was optically projected onto the ISC array. The parallel configuration yielded three output currents I_m, calculated as

$$I_m = \sum_{i=1}^{3}\sum_{j=1}^{3} I_m = \sum_{i=1}^{3}\sum_{j=1}^{3} P_{ij} \cdot R_{m,ij} \tag{1}$$

where $R_{m,ij}$ denotes the photoresponsivity of the m-th subpixel in the (i,j)-th pixel, and P_{ij} is the local light intensity. The resulting currents I_{m} were processed by three sigmoid-type NAF devices to yield output values (f_1, f_2, and f_3), representing the predicted classification probabilities for the three patterns. After each epoch, the prediction results $\hat{y}_k$ were compared with the true labels y_k, and the cross-entropy loss function $\mathcal{L}$ was computed. The gradient was back-propagated to update the photoresponsivity values

$$\Delta R_{m,ij} = \frac{\eta}{S}\sum_{k=1}^{S} \nabla_{R_{m,ij}} \mathcal{L}_k \tag{2}$$

$$\mathcal{L} = -\sum_{k=1}^{M} y_k \log \hat{y}_k \tag{3}$$

where η = 0.2 is the learning rate, and S = 20 denotes the mini-batch size. The field-programmable gate array (FPGA), integrated on the same printed circuit board (PCB) (fig. S48), performed the gradient computations and coordinated with the multiplexer (MUX) array to deliver targeted voltage pulses for selective in situ updates of the photoresponsivity values, enabling efficient online learning (note S4.1). After each training epoch, classification accuracy was evaluated by projecting test images onto the system and analyzing the corresponding output probabilities.

For the traffic-sign recognition task, 14 categories of images from the Kaggle Traffic-Signs Dataset were resized to 32 × 32 pixels (fig. S57). A neural network comprising one convolution layer with three 3 × 3 kernels and three fully connected layers (2700-256-14) was implemented on the Fe-FET hardware. The convolution kernels were mapped to the ISC-mode Fe-FET array, and the fully connected layers were mapped to the IMC-mode array. ReLU-configured Fe-FETs were used for nonlinear activation in both the convolution

layer and the hidden FC layer, while sigmoid-configured Fe-FETs generated the final output activations. During inference, each input image was partitioned into sequential 3 × 3 patches and projected onto the ISC array using an FPGA-controlled SLM. The resulting photocurrents were amplified and passed directly to the ReLU-mode devices (fig. S58), and then to the IMC array for analog MAC operations. Intermediate feature vectors were temporarily stored in the FPGA to accommodate the finite array size. Offline-trained weights were written into the hardware after each epoch via ferroelectric polarization programming. The complete pipeline—ISC convolution, ReLU activation, IMC computation, and sigmoid output—was executed in this manner for all traffic-sign samples.

Reconfigurable Fe-FET–based hardware-level simulation for UA-DETRAC traffic-video processing

We established a hardware-level simulation framework to evaluate how a reconfigurable Fe-FET array could execute traffic-video inference on real surveillance data from the UA-DETRAC dataset. The input is a short video clip represented as a tensor $X \in \mathbb{R}^{B\times10\times3\times64\times64}$, where B is the batch size, 10 denotes the number of frames per clip, and each frame is a 64 × 64 RGB image. As illustrated in fig. S60, the network is organized as an ISC-ReLU-IMC-ReLU-…-IMC-sigmoid pipeline to preserve analog continuity across sensory encoding, linear accumulation, and nonlinear transformation. At the front end, an ISC convolutional stem performs feature extraction directly on the incident frames using 32 kernels of size 3 × 3. In the hardware mapping, this stage is represented by photoresponsivity-coded sensing weights and produces feature-encoded analog photocurrent outputs. The stem output is then passed through a ReLU-type nonlinear activation to introduce the first nonlinearity and suppress negative responses, enabling robust feature propagation. Deep feature extraction is implemented by a sequence of IMC blocks that map the four stages of an SE-ResNet backbone. These stages progressively increase the channel dimension from 64 to 512 while reducing spatial resolution via strided 3 × 3 convolutions. Each convolution or linear operator is expressed as an analog MVM with conductance-coded weights in the IMC array. ReLU activations are interleaved between IMC operators to maintain representational separability and stabilize signal dynamics across stages. Within each IMC stage, a Squeeze-and-Excitation (SE) module is included to recalibrate channel-wise responses. Global average pooling is applied to each channel to form a compact descriptor, followed by a sigmoid gating function with reduction ratio $r = 16$ to generate channel-wise scaling factors. In the hardware abstraction, the linear projections are mapped to IMC operations, and the gating nonlinearity is mapped to a sigmoid-type NAF. Last, a frame-level classifier produces per-frame logits, and a temporal fusion layer aggregates information across the 10-frame clip to output a class-probability vector for traffic-scene/vehicle recognition. In the system-level evaluation, hardware nonidealities and bandwidth constraints are incorporated using the experimentally extracted device and circuit parameters (e.g., Fe-FET response time, programming/readout conditions, and transimpedance amplifier (TIA)-limited throughput), enabling a performance projection of latency and energy under realistic mixed-signal constraints.

Implementation of autoencoding on hardware neuromorphic vision system

The hardware-implemented autoencoder system is schematically shown in fig. S62. It comprises a 3 × 3 × 3 CNN based on ISC operations, a 3 × 9 artificial neural network (ANN) using IMC processing, as well as three ReLU-type and nine sigmoid-type NAF devices. The initial weights, i.e., the photoresponsivity values of the ISC devices and the conductance states of the IMC array, were randomly initialized (fig. S63). During each training epoch, 3 × 3–pixel images containing Gaussian noise were selected from the training dataset and optically projected onto the ISC array. This yielded three photocurrent outputs I_m (m = 1, 2, 3). These currents were passed through three ReLU-type NAF devices, providing nonlinearly activated outputs, which were subsequently converted into voltage signals and routed into the 3 × 9 IMC array (fig. S50). The nine resulting output signals were further processed by nine sigmoid-type NAF devices, producing the reconstructed 3 × 3–pixel output image. The reconstruction error was evaluated using the mean square error loss function

$$\mathcal{L} = \sum_{i=1}^{3}\sum_{j=1}^{3}\left(P_{i,j} - P'_{i,j}\right)^2 \tag{4}$$

where $P_{i,j}$ and $P'_{i,j}$ represent the pixel intensities of the original and reconstructed images at position (i,j), respectively. Gradient-based backpropagation was implemented using the on-board FPGA to compute the error derivatives. Based on the computed gradients, the FPGA coordinated with the analog MUX array to apply targeted electrical pulses, updating the photoresponsivity of the ISC devices and the conductance of the IMC devices after each epoch (note S4.1). This configuration enabled real-time in situ training and reconstruction entirely within the hardware framework.

Supplementary Materials

This PDF file includes:

Figs. S1 to S65
Supplementary Notes S1 to S4
Tables S1 and S2
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